and separate from a tunnel oxide disposed between said source and drain.

REMARKS

Claims 1-7 stand rejected under 35 U.S.C. §112. The Examiner finds the claims to lack clarity.

With regard to the objection to claims 1 and 5, Applicants generally disagree with the Examiner's contention that the specification indicates that the silicon nanoparticles could not be deposited by implantation. In fact, the portion of the specification on page 11 likens a preferred embodiment fabrication process to ion implantation, while noting that it is more similar to a deposit. In either case, the specification is not intended to limit the particular manner by which the silicon nanoparticles are formed into the structure which is claimed in the application. The portion of page 11 simply concerns exemplary preferred formation processes, and draws parallels to some typically used processes. The claims have been amended as the claims were never intended to conjure up product-by-process limitations. The Examiner's point on this issue is well taken, and the claims are amended to make clear that it is the structure which Applicants are claiming and that Applicants are not intending to limit the claims to any particular fabrication process.

The Examiner also found objectionable the recitation "gate area". Applicants believe this would have been understood by ordinary artisans as the specification notes that

the silicon nanoparticles are deposited as a buried gate layer and would understand the general arrangement of the transistors. While a rejection is not believed proper, the recitations have been amended to expedite prosecution.

The Examiner also objects to the term "energy spacing" in claim 4. However, the energy spacing term is explained on page 8 in the first paragraph. Applicants are uncertain what the Examiner finds unclear in view of the definition of energy spacing within the specification. If this rejection is maintained, further explanation is requested.

The Examiner also objects to the use of "electron hole" in claim 5. As indicated in the art in general, and explained in the specification, the electron hole is simply the absence of an electron where otherwise expected. This term is widely used in the applicable art, and is believed to be understood by artisans. A hole is the absence of an electron. Apparently, the Examiner views these terms as being unusable together, so the recitation has simply been replaced with "hole" in claims 5-7.

Claims 1, 3, 5, and 8 stand rejected based upon either Chen or Tiwari which concern similar disclosures. The rejection is respectfully traversed. While these references disclose a transistor using a similar concept, the present invention is distinguished by its use of one nanometer diameter silicon nanoparticles.

The rejection made by the Examiner states that "the diameter of the nanoparticles may be 1 to 2 nanometer" using reference to column 4, line 55 of the Chen patent. That statement of the Examiner is clearly not supported by the Chen patent, which

only discloses layer thicknesses of 1 nanometer and does not disclose any silicon nanoparticles having a 1 nanometer diameter. A 1 nanometer thick layer in Chen will have an area that is greater than 1 nanometer in width and length. Nowhere does Chen state a capability to produce 1 nanometer particles.

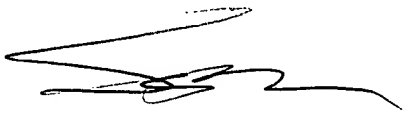
In column 4, Chen explains that "nanocrystal 34 is distinguished from a common or generic layer of semiconductor material in that the nanocrystal is physically confined in three dimensions, each dimension for example, height, width and depth being equal to or less than 40 nm". Later in column 4, Chen describes embodiments with reference to Fig. 1 and Fig. 2 that may have a 1 nanometer thick quantum dot layer. This layer is illustrated in Fig. 2 as having greater width and depth, respectively indicated as 8 nanometers and 20 nanometers. The assumption that a 1 nanometer thick layer is constructed of 1 nanometer particles is fundamentally flawed. The invention concerns and uses silicon particles having a 1nm diameter. A quantum dot, as in Chen, is simply a thin layer. Chen concerns such a thin layer, but provides absolutely no teaching of 1 nanometer diameter particles. Bulk silicon may be deposited as a 1nm thin layer, as in Chen, but is not 1nm diameter particles. Accordingly, the rejections based upon Chen and Tiwari should be withdrawn. The rejections that borrow from Chen and Tiwari should also be withdrawn.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached Appendix is captioned "**Version with markings to show changes made.**"

For the foregoing reasons, applicant believes that this case is in condition for allowance, which is respectfully requested. The examiner should call applicants' attorney if an interview would expedite prosecution.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Please cancel claim 3 and amend claims 1, 5, 6, 7 and 8 as follows:

1. (Amended) A single electron transistor device comprising:

a source;

a drain;

a gate [having a gate area; and] ;

a buried gate layer of silicon nanoparticles [implanted in said gate area.] ; and

wherein said silicon nanoparticles have a diameter of approximately 1 nm.

5. (Amended) A method for operating a single electron device, which has a source, a drain, a gate [having a gate area], and [at least] 1nm diameter silicon nanoparticles implanted [in the gate area] as a buried gate layer, comprising the steps of:

creating at least one [electron] hole in the silicon nanoparticles to enable the silicon nanoparticles to conduct a single electron at room temperature across the source and the drain; and

applying a voltage across the drain and the source.

6. (Amended) The method of operating the single electron device according to claim 4, wherein said step of creating [an electron] a hole in said silicon nanoparticles is accomplished by irradiating said silicon nanoparticles.

7. (Amended) The method of operating the single electron device according to claim 5, wherein said step of creating [an electron] a hole uses light having a spectral width between 300nm and 600nm.

8. (Amended) A transistor memory device comprising:

a source;

a drain; and

a gate, [said gate having a gate area] with 1nm diameter silicon nanoparticles contained in a control oxide and separate from a tunnel oxide disposed between said source and drain.